Listing Of Claims

1. (Withdrawn) An array substrate for in-plane switching liquid crystal display device, comprising:

a gate line arranged in a transverse direction on a substrate, the gate line including a gate electrode;

a data line arranged in a direction substantially perpendicular to the gate line, the data line including a source electrode;

a common line arranged parallel with the gate line, the common line including a plurality of common electrodes;

a gate insulation layer on the substrate, the gate insulation layer covering the gate line, the gate electrode, the common line and the plurality of common electrodes;

a semiconductor layer on the gate insulation layer;

a plurality of pixel electrodes arranged substantially parallel with the data line;

a drain electrode spaced apart from the source electrode; and

an alignment layer on the plurality of pixel electrodes and the source and drain electrodes, whereby the alignment layer protects the pixel electrodes and the source and drain electrodes.

2. (Withdrawn) The device of claim 1, wherein the gate electrode, the semiconductor layer, the source electrode and the drain electrode form a thin film transistor.

3. (Withdrawn) The device of claim 2, wherein the thin film transistor is disposed at the crossing of the gate and data lines.

4. (Withdrawn) The device of claim 1, wherein the gate insulation layer is one of benzocyclobutene (BCB) and acryl-based resin.

5. (Withdrawn) The device of claim 1, wherein the alignment layer is one of polyimide and polyamide.

6. (Withdrawn) The device of claim 1, wherein the gate line and the common line include at least aluminum.

7. (Withdrawn) The device of claim 1, wherein the data line and the plurality of pixel electrodes are formed of one of molybdenum (Mo), tungsten (W) and chromium (Cr).

8. (Withdrawn) The device of claim 1, wherein the semiconductor layer includes an active layer and an ohmic contact layer.

9. (Withdrawn) The device of claim 1, further comprising a pixel connecting line substantially parallel with the gate line.

10. (Withdrawn) The device of claim 9, wherein the drain electrode is connected to the pixel connecting line.

11. (Withdrawn) The device of claim 9, wherein the pixel connecting line connects the plurality of pixel electrodes to each other.

12. (Currently Amended) A method of forming an array substrate for an in-plane switching liquid crystal display device, the method comprising:

forming a first metal layer on a substrate;

patterning the first metal layer using a first mask to form a gate line having a gate electrode and a common line having a plurality of common electrodes;

forming a gate insulation layer on the substrate to cover the patterned first metal layer;

forming a semiconductor layer on the gate insulation layer using a second mask;

forming a second metal layer on the gate insulation layer to cover the semiconductor layer;

patterning the second metal layer using a third mask to form a data line having a source electrode, a pixel connecting line connecting a plurality of pixel electrodes, and a drain electrode that is spaced apart from the source electrode;

forming a channel by etching a portion of the ~~ohmic contact~~ semiconductor layer between the source and drain electrodes;

forming an alignment layer over the substrate to cover the patterned second metal layer; and

simultaneously thermal-treating the ~~substrate having the~~ alignment layer and the source and drain electrode.

13. (Original) The method of claim 12, wherein the thermal treatment is performed at a temperature of 200 to 230 degrees centigrade.

14. (Original) The method of claim 13, wherein the thermal treatment is maintained for about 2 to 3 hours in a furnace.

15. (Original) The method of claim 12, further comprising curing the alignment layer during the thermal treatment.

16. (Original) The method of claim 15, further comprising annealing a thin film transistor including the source and drain electrodes, the gate electrode and the semiconductor layer.

17. (Original) The method of claim 16, wherein the curing and annealing are contemporaneous.

18. (Original) The method of claim 12, wherein the alignment layer is cured through the thermal treatment.

19. (Original) The method of claim 12, wherein a thin film transistor including the gate electrode, the semiconductor layer and the source and drain electrodes are annealed during the curing process of the alignment layer.

20. (Original) The method of claim 12, wherein the alignment layer protects the source and drain electrodes, the gate electrode and the semiconductor layer.

21. (Original) The method of claim 12, wherein a thin film transistor includes the source and drain electrodes, the gate electrodes and the semiconductor layer.

22. (Original) The method of claim 21, wherein the alignment layer protects the thin film transistor.

23. (Original) The method of claim 12, wherein the semiconductor layer includes an active layer and an ohmic contact layer.

24. (Original) The method of claim 12, further comprising rubbing the alignment layer.

25. (Original) The method of claim 24, wherein the rubbing direction is about 5 to about 45 degrees from the common and pixel electrodes.